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# CubeSat Kit™

Pluggable Processor Module (PPM) A3  
Hardware Revision: B

## PPM with TI's MSP430F2618 for CubeSat Kit Motherboard

### Applications

- CubeSat nanosatellite control, C&DH, TT&C
- General-purpose low-power computing for CubeSat Kit architecture
- Remote sensing for harsh environments

### Features

- For CubeSat Kit Motherboard (MB)
- TI's MSP430F2618 16-bit microcontroller (MCU)
- 116KB program memory, 8KB on-chip SRAM
- Integrated peripherals:
  - 2 USCI\_A (UARTA0/SPIA0 & UARTA1/SPIA1)
  - 2 USCI\_B (I2CB0/SPIB0 & I2CB1/SPIB1)
  - 8-channel 12-bit ADC
  - 2-channel 12-bit DAC
  - 16-bit Timer\_A3
  - 16-bit Timer\_B7
  - 3-channel DMA
  - On-chip comparator
  - SVS, BOR, WDT, JTAG, etc.
- 7.3728MHz & 32.768kHz clock crystals
- PCA9515A I2C isolator
- Ultra-low power operation
- Independent latchup (device overcurrent) protection
- Independent external reset supervisor (POR/BOR)
- Small-size PPM footprint
- 4-layer gold-plated blue-soldermask PCB
- Compatible with Pumpkin's Salvo™ RTOS and HCC-Embedded's EFFS-THIN SD Card file FAT file system for ease of programming



### ORDERING INFORMATION

Pumpkin P/N 710-00516

Option Code	PPM Connector Height
/00 (standard)	+3mm

Contact factory for availability of optional configurations.  
Option code /00 shown.



### CAUTION

Electrostatic  
Sensitive  
Devices

Handle with  
Care



**CHANGELOG**

Rev.	Date	Author	Comments
A	20090728	AEK	Initial revision.
B	20090808	AEK	Added photo.
C	20100113	AEK	Revised I <sub>SLEEP</sub> based on lot testing of PCA9515A.

## OPERATIONAL DESCRIPTION

PPM A3 enables CubeSat Kit customers to utilize TI's ultralow-power MSP430 processor on a CubeSat Kit Motherboard (MB). PPM A3 uses the 64-pin MSP430F2618TPM, with a wide selection of on-chip peripherals. Additionally, a PCA9515A I2C isolator is present to facilitate I2C interfacing and simple backwards compatibility with PPM A1 and PPM A2.

The MSP430F2618 employs the MSP430X core architecture – an extension of the 16-bit MSP430 architecture to 20 bits of address space. Tools capable of supporting the MSP430X architecture must be used to take advantage of the 20-bit address space.

## ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Operating temperature	$T_A$	-40 to +85	°C
Voltage on +5V_USB bus		-0.3 to +6.0	V
Voltage on +5V_SYS bus			
Voltage on -FAULT_OC open-collector output			
Voltage on VCC bus		-0.3 to +3.6	V
Voltage on VCC_SD bus			
Voltage on any MSP430 I/O pin		-0.3 to 3.6	V
Diode current at any MSP430 pin		-2 to +2	mA
DC current through any pin of PPM connector H1	$I_{PIN\_MAX}$	1.2	A
MSP430 operating frequency	$f_{OP\_MAX}$	16	MHz

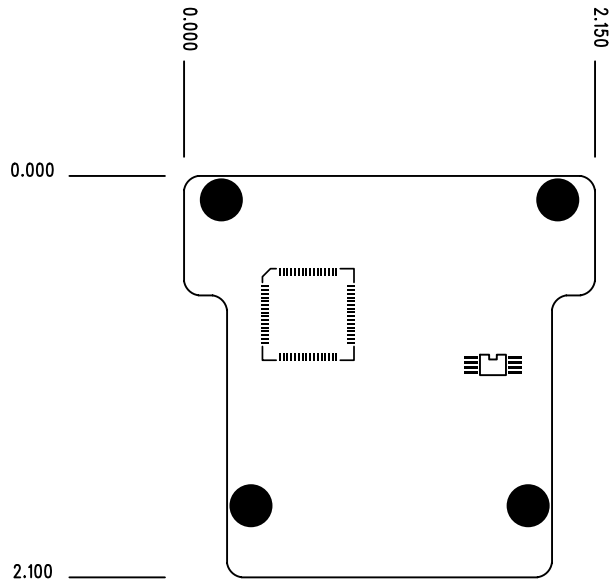
Refer to the MSP430x261x family datasheet for additional absolute maximum ratings associated with processor U1, especially per-pin current limits.

**PHYSICAL CHARACTERISTICS**

Parameter	Conditions / Notes	Symbol	Min	Typ	Max	Units
Mass				11		g
Height of components above PCB					2	mm
Height of components below PCB <sup>1</sup>					4	mm
PCB width	Small-size PPM			54.6		mm
PCB length				53.4		mm
PCB thickness				1.6		mm

**SIMPLIFIED MECHANICAL LAYOUT<sup>2</sup>**

PPM A3 is implemented on a small-size PPM PCB, as shown below.



<sup>1</sup> Not including connector H1.

<sup>2</sup> Dimensions in inches.

**ELECTRICAL CHARACTERISTICS**

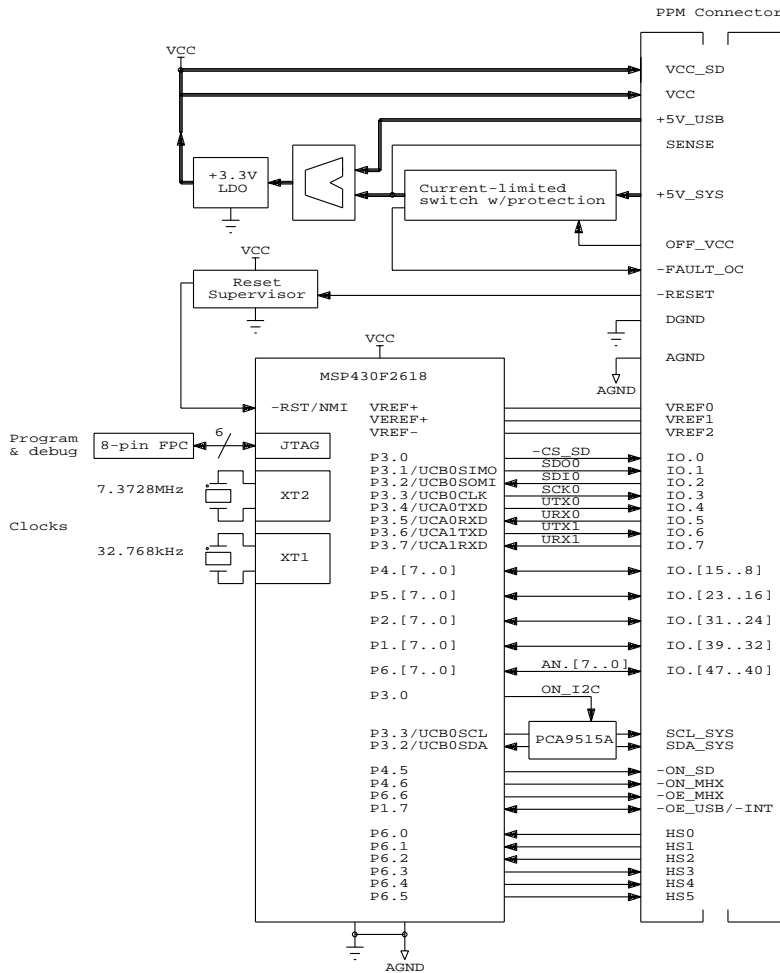
(T = 25°C, +5V bus = +5V unless otherwise noted)

Parameter	Conditions / Notes	Symbol	Min	Typ	Max	Units
Reset voltage	+5V_SYS reduced until MCU resets	V <sub>RESET_MAX</sub>			3.1	V
Operating Voltage		V <sub>CC</sub>		3.3		V
SD Card Voltage		V <sub>CC_SD</sub>		3.3		V
Operating current	LPM0, MCLK = DCO	I <sub>OP</sub>		3		mA
	LMP4, all control outputs inactive, I2C isolator U5 fitted	I <sub>SLEEP</sub>	400		1000	µA
	LMP4, all control outputs inactive, I2C isolator U5 not fitted			33	40	µA
Low-frequency clock frequency	LFXTAL	f <sub>CLK_LF</sub>	32.768 ± 0.001			kHz
DCO clock frequency	DCOCLK	f <sub>CLK_DCO</sub>	680	760	840	kHz
High-frequency clock frequency	HFXTAL	f <sub>CLK_HF</sub>	7.3728 ± 0.0005			MHz
Overcurrent trip point for VCC	Set by R3	I <sub>TRIP_VCC</sub>		220		mA
Time to switch between +5V_SYS and +5V_USB power sources	Automatic				1	µs

For more information on TI's MSP430 ultralow-power microcontrollers, refer to the TI datasheets.

## BLOCK DIAGRAM

PPM A3 provides regulated and current-limited +3.3V power, an external POR/BOR reset supervisor, a JTAG interface for programming and debugging, two clock sources, an external I2C isolator, connections to all 48 I/O pins of the PPM connector, shared MB control and radio handshaking signals, and a single-point analog/digital ground. All of the 64-pin MSP430's pin are used, some for multiple purposes.



## PPM PIN DESCRIPTIONS

The PPM connector H1 connects the PPM to resources residing on the MB and to resources accessible via the CubeSat Kit Bus connector.<sup>3</sup>

Those signals that are connected directly to the PPM connector and to the CubeSat Kit Bus connectors are tagged under the CSKB label below.<sup>4</sup> Signals marked with an ‘\*’ are associated with dedicated peripherals on the MB. Some may also be used with off-board peripherals through the proper use of MB peripheral enables and MB power control.

The *potential* for a pin’s function is described by the I/O field. The *recommended usage* (as a digital or analog input or output, or as a power pin) is listed in the Description field. I/O pins can generally be configured as general-purpose I/O if the recommended usage is not desired.

*Inputs* are signals *from* the MB to the PPM’s processor U1 or other circuitry. *Outputs* are signals *from* the PPM’s processor U1 or other circuitry *to* the MB.

		H1			
		LSS-150-01-L-DV			
IO.23	2	1	IO.47		
IO.22	4	3	IO.46		
IO.21	6	5	IO.45		
IO.20	8	7	IO.44		
IO.19	10	9	IO.43		
IO.18	12	11	IO.42		
IO.17	14	13	IO.41		
IO.16	16	15	IO.40		
IO.15	18	17	IO.39		
IO.14	20	19	IO.38		
IO.13	22	21	IO.37		
IO.12	24	23	IO.36		
IO.11	26	25	IO.35		
IO.10	28	27	IO.34		
IO.9	30	29	IO.33		
IO.8	32	31	IO.32		
IO.7	* 34	33	IO.31		
IO.6	* 36	35	IO.30		
IO.5	* 38	37	IO.29		
IO.4	* 40	39	IO.28		
IO.3	* 42	41	IO.27		
IO.2	* 44	43	IO.26		
IO.1	* 46	45	IO.25		
IO.0	* 48	47	IO.24		
+5V_USB	50	49	+5V_USB		
+5V_SYS	52	51	+5V_SYS		
VCC_SD	54	53	VCC_SD		
VCC	56	55	VCC		
DGND	58	57	DGND		
AGND	60	59	AGND		
VBATT	62	61	VBATT		
VBACKUP	64	63	VBACKUP		
VREF0	66	65	* -FAULT_OC	<--	
VREF1	68	67	SENSE	<--	
VREF2	70	69	-RESET	-->	
	X	72	OFF_VCC	-->	
	X	74	SDA_SYS	<-->	
	X	76	SCL_SYS	<-->	
	X	78			
	X	80			
--> -ON_SD	* 82	81			
--> -ON_MHX	* 84	83			
--> -OE_MHX	* 86	85			
--> -OE_USB/-INT	* 88	87			
<-- HS0	* 90	89			
<-- HS1	* 92	91			
<-- HS2	* 94	93			
--> HS3	* 96	95			
--> HS4	* 98	97			
--> HS5	* 100	99			

<sup>3</sup> Not included. MBs are purchased separately from PPMs.

<sup>4</sup> The CubeSat Kit’s system peripherals are numbered from 0 onwards (e.g., U0, SPI0, etc.), and this nomenclature is used when referring to a PPM or CSK bus signal. The MSP430’s peripheral nomenclature begins with 0 (e.g., UART0, SPI0, etc.), and is used when referring to peripherals, signals and registers internal to the MSP430.

## PPM PIN DESCRIPTIONS – I/O

Name	Pin	I/O	CSKB	Description
IO.0	H1.48	I/O	•	-CS_SD/ON_I2C. Controls SD Card interface and I2C isolator. From P3.0 (U1.28). Part of the MB's SD card interface and the PPM's I2C isolator. P3.0 is normally configured as a simple digital output.
IO.1	H1.46	I/O	•	SDO0. SPI0 (master) data out. From P3.1/UCB0SIMO (U1.29). Part of the MB's SD card interface. P3.1/UCB0SIMO is normally configured as a digital output as part of UCB0:SPI when the SPI peripheral is active.
IO.2	H1.44	I/O	•	SDI0. SPI0 (master) data in. To P3.2/UCB0SOMI (U1.30). Part of the MB's SD card interface. P3.2/UCB0SOMI is normally configured as a digital input as part of UCB0:SPI when the SPI peripheral is active.
IO.3	H1.42	I/O	•	SCK0. SPI0 clock. From P3.3/UCB0CLK (U1.31). Part of the MB's SD card interface. P3.3/UCB0CLK is normally configured as a digital output as part of UCB0:SPI when the SPI peripheral is active.
IO.4	H1.40	I/O	•	UTX0. Tx0 data out. From P3.4/UCA0TXD (U1.32). P3.4/UCA0TXD is normally configured as a digital output as part of UCA0:UART when the UART peripheral is active.
IO.5	H1.38	I/O	•	URX0. Rx0 data in. To P3.5/UCA0RXD (U1.33). P3.5/UCA0RXD is normally configured as a digital input as part of UCA0:UART when the UART peripheral is active.
IO.6	H1.36	I/O	•	UTX1. Tx1 data out. From P3.6/UCA1TXD (U1.34). Part of the MB's MHX/USB interface. P3.6/UCA1TXD is normally configured as a digital output as part of UCA1:UART when the UART peripheral is active.
IO.7	H1.34	I/O	•	URX1. Rx1 data in. To P3.7/UCA1RXD (U1.35). Part of the MB's MHX/USB interface. P3.7/UCA1RXD is normally configured as a digital input as part of UCA1:UART when the UART peripheral is active.
IO.8	H1.32	I/O	•	General-purpose I/O. To/from P4.0 (U1.36).
IO.9	H1.30	I/O	•	General-purpose I/O. To/from P4.1 (U1.37).
IO.10	H1.28	I/O	•	General-purpose I/O. To/from P4.2 (U1.38).
IO.11	H1.26	I/O	•	General-purpose I/O. To/from P4.3 (U1.39).
IO.12	H1.24	I/O	•	General-purpose I/O. To/from P4.4 (U1.40).
IO.13	H1.22	I/O	•	-ON_SD. MB control signal. From P4.5 (U1.41). Part of the MB's SD card interface. P4.5 is normally configured as a digital output. See -ON_SD signal description, below.
IO.14	H1.20	I/O	•	-ON_MHX. MB control signal. From P4.6 (U1.42). Part of the MB's MHX interface. P4.6 is normally configured as a digital output. See -ON_MHX signal description, below.
IO.15	H1.18	I/O	•	General-purpose I/O. To/from P4.7 (U1.43).
IO.16	H1.16	I/O	•	General-purpose I/O. To/from P5.0 (U1.44).
IO.17	H1.14	I/O	•	General-purpose I/O. To/from P5.1 (U1.45).
IO.18	H1.12	I/O	•	General-purpose I/O. To/from P5.2 (U1.46).
IO.19	H1.10	I/O	•	General-purpose I/O. To/from P5.3 (U1.47).
IO.20	H1.8	I/O	•	General-purpose I/O. To/from P5.4 (U1.48).
IO.21	H1.6	I/O	•	General-purpose I/O. To/from P5.5 (U1.49).
IO.22	H1.4	I/O	•	General-purpose I/O. To/from P5.6 (U1.50).
IO.23	H1.2	I/O	•	General-purpose I/O. To/from P5.7 (U1.51).
IO.24	H1.47	I/O	•	General-purpose I/O. To/from P2.0 (U1.20).
IO.25	H1.45	I/O	•	General-purpose I/O. To/from P2.1 (U1.21).
IO.26	H1.43	I/O	•	General-purpose I/O. To/from P2.2 (U1.22).

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IO.27	H1.41	I/O	•	General-purpose I/O. To/from P2.3 (U1.23).
IO.28	H1.39	I/O	•	General-purpose I/O. To/from P2.4 (U1.24).
IO.29	H1.37	I/O	•	General-purpose I/O. To/from P2.5 (U1.25).
IO.30	H1.35	I/O	•	General-purpose I/O. To/from P2.6 (U1.26).
IO.31	H1.33	I/O	•	General-purpose I/O. To/from P2.7 (U1.27).
IO.32	H1.31	I/O	•	General-purpose I/O. To/from P1.0 (U1.12).
IO.33	H1.29	I/O	•	General-purpose I/O. To/from P1.1 (U1.13).
IO.34	H1.27	I/O	•	General-purpose I/O. To/from P1.2 (U1.14).
IO.35	H1.25	I/O	•	General-purpose I/O. To/from P1.3 (U1.15).
IO.36	H1.23	I/O	•	General-purpose I/O. To/from P1.4 (U1.16).
IO.37	H1.21	I/O	•	General-purpose I/O. To/from P1.5 (U1.17).
IO.38	H1.19	I/O	•	General-purpose I/O. To/from P1.6 (U1.18).
IO.39	H1.17	I/O	•	<i>-OE_USB/-INT</i> . MB control/status signal. To/from P1.7 (U1.19). <i>Part of the MB's USB and RTC interfaces. P1.7 is normally configured as a digital output. See -OE_USB and -INT signal descriptions, below.</i>
IO.40	H1.15	I/O	•	<i>AN.0/HS0</i> . Analog input or MB handshake signal. To/from P6.0 (U1.59). <i>Part of the MB's MHX interface. P6.0 is normally configured as a digital input. See HS0 signal description, below. Can also be used as a general-purpose I/O or an analog input.</i>
IO.41	H1.13	I/O	•	<i>AN.1/HS1</i> . Analog input or MB handshake signal. To/from P6.1 (U1.60). <i>Part of the MB's MHX interface. P6.1 is normally configured as a digital input. See HS1 signal description, below. Can also be used as a general-purpose I/O or an analog input.</i>
IO.42	H1.11	I/O	•	<i>AN.2/HS2</i> . Analog input or MB handshake signal. To/from P6.2 (U1.61). <i>Part of the MB's MHX interface. P6.2 is normally configured as a digital input. See HS2 signal description, below. Can also be used as a general-purpose I/O or an analog input.</i>
IO.43	H1.9	I/O	•	<i>AN.3/HS3</i> . Analog input or MB handshake signal. To/from P6.3 (U1.2). <i>Part of the MB's MHX interface. P6.3 is normally configured as a digital output. See HS3 signal description, below. Can also be used as a general-purpose I/O or an analog input.</i>
IO.44	H1.7	I/O	•	<i>AN.4/HS4</i> . Analog input or MB handshake signal. To/from P6.4 (U1.3). <i>Part of the MB's MHX interface. P6.4 is normally configured as a digital output. See HS4 signal description, below. Can also be used as a general-purpose I/O or an analog input.</i>
IO.45	H1.5	I/O	•	<i>AN.5/HS5</i> . Analog input or MB handshake signal. To/from P6.5 (U1.4). <i>Part of the MB's MHX interface. P6.5 is normally configured as a digital output. See HS5 signal description, below. Can also be used as a general-purpose I/O or analog input.</i>
IO.46	H1.3	I/O	•	<i>AN.6/-OE_MHX</i> . Analog input or MB control signal. To/from P6.6 (U1.5). <i>Part of the MB's MHX interface. P6.6 is normally configured as a digital output. See -OE_MHX signal description, below. Can also be used as general-purpose I/O or an analog output.</i>
IO.47	H1.1	I/O	•	<i>AN.7</i> . Analog input. To/from P6.7 (U1.6). <i>Can also be used as a general-purpose I/O or an analog output.</i>

**PPM PIN DESCRIPTIONS – Power**

Name	Pin	I/O	CSKB	Description
+5V_USB	H1.49 H1.50	–	•	+5V USB power. From USB host. Powers PPM.
+5V_SYS	H1.51 H1.52	–	•	+5V system power. From EPS or external +5V connector. Powers PPM.
VCC_SD	H1.53 H1.54	–		+3.3V SD Card power. From PPM's vcc.
VCC	H1.55 H1.56	–		+3.3V PPM power, MB power and I/O level. From PPM LDO U4 using +5V_SYS and/or +5V_USB.
DGND	H1.57 H1.58	–	•	Digital ground.
AGND	H1.59 H1.60	–	•	Analog ground.
VBATT	H1.61 H1.62	–	•	Not connected.
VBACKUP	H1.63 H1.64	–	•	Not connected.

**PPM PIN DESCRIPTIONS – Analog References**

Name	Pin	I/O	CSKB	Description
VREF0	H1.66	–	•	Positive analog voltage reference. To/from VREF+ (U1.7).
VREF1	H1.68	–	•	Positive analog voltage reference. To/from VREF+ (U1.10).
VREF2	H1.70	–	•	Negative analog voltage reference. To/from VREF- (U1.11).

**PPM PIN DESCRIPTIONS – Reserved**

Name	Pin	I/O	CSKB	Description
RSVD0	H1.72	–	•	Not connected. Reserved for future use.
RSVA1	H1.74	–	•	Not connected. Reserved for future use.
RSVD2	H1.76	–	•	Not connected. Reserved for future use.

**PPM PIN DESCRIPTIONS – MB-Specific**

Name	Pin	I/O	CSKB	Description
CB4 USBDP	H1.78	I		Not connected.
CB2 USBDM				
-ON_SD	H1.82	O		Control signal for SD Card power. From P4.5 (U1.41). Active LOW, pulled high on the MB. When active, enables VCC_CARD on the MB, thereby powering SC Card socket and SD Card level translators / isolators. <i>Normally configured as a digital output.</i>
-ON_MHX	H1.84	O		Control signal for MHX socket power. From P4.6 (U1.42). Active LOW, pulled high on the MB. When active, enables PWR_MHX on the MB, thereby powering MHX socket and MHX level translators / isolators. <i>Normally configured as a digital output.</i>
-OE_MHX	H1.86	O		Control signal for MHX interface. From P6.6 (U1.5). Active LOW, pulled high on the MB. When active, enables signals to pass through MHX level translators / isolators. <i>Normally configured as a digital output.</i>
-OE_USB	H1.88	O		Control signal for USB interface. From P1.7 (U1.19). Active LOW, pulled high on the MB. When active, enables signals to pass through USB level translators / isolators. <i>Normally configured as a digital output.</i>

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<b>-INT</b>		I		Output from RTC's -IRQ open-collector output. To P1.7 (U1.19). When properly configured, can be used to interrupt processor U1 via MB RTC. <i>Normally configured as a digital input.</i>
<b>HS0</b>	H1.90	I		Handshake signal. -RTS (USB) or -CTS (MHX). To P6.0 (U1.59). <i>Normally configured as a digital input. Requires that R10 be fitted on the MB.</i>
<b>HS1</b>	H1.92	I		Handshake signal. -DTR (USB) or -DSR (MHX). To P6.1 (U1.60). <i>Normally configured as a digital input. Requires that R11 be fitted on the MB.</i>
<b>HS2</b>	H1.94	I		Handshake signal. -PWE (USB) or -DCD (MHX). To P6.2 (U1.61). <i>Normally configured as a digital input. Requires that R12 be fitted on the MB.</i>
<b>HS3</b>	H1.96	O		Handshake signal. -CTS (USB) or -RTS (MHX). From P6.3 (U1.2). <i>Normally configured as a digital output. Requires that R75 be fitted on the MB.</i>
<b>HS4</b>	H1.98	O		Handshake signal. -RI (USB) or -DTR (MHX). From P6.4 (U1.3). <i>Normally configured as a digital output. Requires that R76 be fitted on the MB.</i>
<b>HS5</b>	H1.100	O		Handshake (reset) signal. -RST (USB) or -RST (MHX). From P6.5 (U1.4). <i>Normally configured as a digital output. Requires that R77 be fitted on the MB.</i>

### PPM PIN DESCRIPTIONS – Control & Status

Name	Pin	I/O	CSKB	Description
<b>-FAULT_OC</b>	H1.65	O		Open-collector output from PPM's latchup prevention overcurrent switch. Active LOW. Wire-ORed to <b>-FAULT_OC</b> on the MB.
<b>SENSE</b>	H1.67	-	•	Can be used to measure PPM's current consumption. The current used by the PPM from a single source is (source – <b>SENSE</b> ) / 75mΩ. Depends on PPM implementation.
<b>-RESET</b>	H1.69	I	•	Reset signal to PPM's reset supervisor. Active LOW.
<b>OFF_VCC</b>	H1.71	I	•	Control signal to PPM's power circuit(s). Active HIGH.

### PPM PIN DESCRIPTIONS – I2C Bus

Name	Pin	I/O	CSKB	Description
<b>SDA_SYS</b>	H1.73	I/O	•	I2C data. To/from P3.1/USB0SDA (U1.29) through I2C isolator U5 when ON_I2C is active. <i>Part of the I2C interface. UCB0SDA is normally configured as an I2C data input/output as part of UCB0:I2C when the I2C peripheral is active.</i>
<b>SCL_SYS</b>	H1.75	O	•	I2C clock. From P3.2/UCB0SCL (U1.30) through I2C isolator U5 when ON_I2C is active. <i>Part of the I2C interface. UCB0SCL is normally configured as an I2C clock output as part of UCB0:I2C when the I2C peripheral is active.</i>

### PPM PIN DESCRIPTIONS – User-defined

Name	Pin	I/O	CSKB	Description
<b>USER0</b>	H1.77	I/O	•	Not connected.
<b>USER1</b>	H1.79	I/O	•	Not connected.
<b>USER2</b>	H1.81	I/O	•	Not connected.
<b>USER3</b>	H1.83	I/O	•	Not connected.
<b>USER4</b>	H1.85	I/O	•	Not connected.
<b>USER5</b>	H1.87	I/O	•	Not connected.
<b>USER6</b>	H1.89	I/O	•	Not connected.
<b>USER7</b>	H1.91	I/O	•	Not connected.

<b>USER8</b>	H1.93	I/O	•	Not connected.
<b>USER9</b>	H1.95	I/O	•	Not connected.
<b>USER10</b>	H1.97	I/O	•	Not connected.
<b>USER11</b>	H1.99	I/O	•	Not connected.

### SHARED I/O PINS

All of U1's I/O pins are connected directly to the CubeSat Kit Bus. Due to the relatively low pincount of the MSP430F2618 used on PPM A3, some of the general-purpose I/O pins are also connected to other signals on PPM connector H1. Generally speaking, these shared I/O pins are dedicated to ancillary functions and should not be used by modules on the CubeSat Kit Bus. Provisions are in place to "free" some of these shared I/O pins from their ancillary functions, as outlined below.

Pin	Signal	Standalone Function	Ancillary Function	Notes
P1.7	-OE_USB/-INT	-OE_USB, -INT	I/O	Always connected to USB interface. Pulled up via 100kΩ to VCC on the MB. Can be isolated from RTC by removal of R73 on the MB. Can be used as simple I/O if VCC_IO is not present on the MB <sup>5</sup> and RTC on the MB is configured to ignore -OE_USB/-INT.
P4.5	-ON_SD	-ON_SD	none	Always connected to SD Card interface. Pulled up via 100kΩ to VCC on the MB. Arbitration with U1 can permit other devices to control the MB's SD Card interface.
P4.6	-ON_MHX	-ON_MHX	I/O	Always connected to MHX power switching. Pulled up via 100kΩ to VCC on the MB. Arbitration with U1 can permit other devices to power an MHX transceiver on the MB. Can be used as I/O if no source of power is available on the MB to power MHX socket.
P6.0	HS0	HS0	I/O, analog input	When R10 on the MB is fitted, to be used as a handshake line to USB or MHX. When R10 on the MB is <i>not</i> fitted, to be used as analog input or digital I/O.
P6.1	HS1	HS1	I/O, analog input	When R11 on the MB is fitted, to be used as a handshake line to USB or MHX. When R11 on the MB is <i>not</i> fitted, to be used as analog input or digital I/O.
P6.2	HS2	HS2	I/O, analog input	When R12 on the MB is fitted, to be used as a handshake line to USB or MHX. When R12 on the MB is <i>not</i> fitted, to be used as analog input or digital I/O.
P6.3	HS3	HS3	I/O, analog input	When R75 on the MB is fitted, to be used as a handshake line to USB or MHX. When R75 on the MB is <i>not</i> fitted, to be used as analog input or digital I/O.
P6.4	HS4	HS4	I/O, analog input	When R76 on the MB is fitted, to be used as a handshake line to USB or MHX. When R76 on the MB is <i>not</i> fitted, to be used as analog input or digital I/O.
P6.5	HS5	HS5	I/O, analog input	When R77 on the MB is fitted, to be used as a handshake line to USB or MHX. When R77 on the MB is <i>not</i> fitted, to be used as analog input or digital I/O.

<sup>5</sup> I.e., if USB is not connected.

<b>P6.6</b>	<b>-OE_MHX</b>	<b>-OE_MHX</b>	<b>I/O</b>	Always connected to MHX interface. Pulled up via 100kΩ to vcc on the MB. Can be used as an analog input, analog output or simple I/O when <b>DPWR_MHX</b> on the MB is off.
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For example, if **-ON\_MHX** is kept inactive, **DPWR\_MHX** on the MB is off. Therefore MB MHX isolators **U2** and **U3** are left in a high-impedance state, and **P6.[7..0]** can all be used as analog inputs, getting their signals from the CubeSat Kit Bus via **IO.[47..40]**.<sup>6</sup> This is true regardless of the state of the resistors **R10-R12** and **R75-R77** on the MB. For further information, consult the PPM A3 and MB schematics.

## I2C ISOLATOR & ALTERNATE I2C CONFIGURATIONS

On PPM A3, **U5** is an I2C bus isolator implemented via a PCA9515A. The purpose of **U5** is to ensure that the I2C peripherals attached to the I2C bus via **SCL\_SYS** and **SDA\_SYS** do not see spurious clock and/or data signals when SPI activity is present on **SPI0**, which might cause problems with the I2C bus. I2C signals to/from **U1** can only reach the I2C bus when **ON\_I2C** is active. Therefore, when **ON\_I2C** is inactive, **U1** can perform SPI activity on **SPI0** (e.g., read from and write to the SD Card on the MB) without fear of I2C bus problems.

PPM A3 is configured at the factory to be a drop-in replacement for PPM A1 or A2 in terms of electrical connectivity. This is done by fitting **R5** instead of **R4** for proper sourcing of the **UCB0SCL** signal to **SCL\_SYS** and by using the MSP430F2618's UCB0:I2C peripheral instead of the MSP430F161x's USART0:I2C peripheral for I2C communications. Different firmware is required for PPM A3, because of its use of the different peripherals involved.

Alternatively, users can employ the UCB1:I2C peripheral instead of the UCB0:I2C peripheral for I2C communications. This has the advantage of no longer requiring an I2C isolator, since the UCB1:I2C peripheral is on **P5.1** and **P5.2**. As long as the user has no SPI devices using the UCB1:SPI peripheral, no I2C isolator is required. To make use of this option, a qualified electronics assembler can remove **U5** and **R4-R7**, and fit **R8-R9**.

**U5** has a quiescent current consumption  $I_{SLEEP}$  of around 500μA, regardless of the state of **ON\_I2C**. This sets the floor for  $I_{SLEEP}$ . Users not requiring I2C connectivity, wishing to implement an I2C isolator elsewhere in the system, or implementing I2C via UCB1 can remove **U5**, thereby reducing  $I_{SLEEP}$  to under 40μA.<sup>7</sup>

## OSCILLATOR OPTIONS AND OPERATING SPEEDS

The MSP430F261x family is rated for 16MHz operating speeds at **vcc = +3.3V**. For maximum backwards compatibility with PPM A1 and A2, a 7.3728MHz crystal is fitted to PPM A3. Users can replace crystal **x3** with a faster crystal<sup>8</sup> using a qualified electronics assembler.

## CONNECTORS

<b>Item</b>	<b>Description</b>	<b>Source</b>	<b>Part Number</b>	<b>Application</b>
1	100-pin, hermaphroditic	Samtec	LSS-150-01-L-DV	PPM connector (standard, +3mm)

This connector information is provided for reference only.

## PROGRAMMING & DEBUGGING

<sup>6</sup> Even if an analog signal drives **P6.6 (-OE\_MHX)** below the input threshold of **U1** or **U2**, the isolators remain in their high-impedance state because **DPWR\_MHX** (enabled via **-ON\_MHX**) is off.

<sup>7</sup>  $I_{SLEEP}$  of 40μA is representative of the quiescent current of the previous-generation FM430 flight module, of which the MB + PPM A3 combination is a superset.

<sup>8</sup> E.g., ECS P/N ECS-160-20-5PXDN.

PPM A3 provides one interface for programming and debugging – the popular and low-cost Flash Emulation Tool (FET) interface, a type of JTAG interface. It is implemented via Flexible Printed Circuit (FPC) connector on the PPM.

8-pin FPC connector J1 is for the FET. Via Pumpkin's JFPC-MSP430 adapter, customers can connect either a traditional TI USB or parallel FET, or an aftermarket FET, all with 14-pin 2x7 0.100" pitch dual-inline headers. The JFPC-MSP430 connects to PPM A3 via an 8-conductor FPC cable.

### NOTES

PPM A3 (MSP430F2618) is built on the same Pumpkin PCB (705-00378) as PPM A1 (MSP430F1612) and PPM A2 (MSP430F1611), with minor differences in the components placed at assembly time.

## TRADEMARKS

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